REMARKS

Claims 1-9 were pending in the application. Applicant adds new claims 10-20. Accordingly, claims 1-20 are now pending in the present application, of which claims 1, 7 and 16 are independent. Favorable consideration of the application, as amended, is respectfully requested.

35 U.S.C. § 102

The Examiner has rejected claims 1 and 7-9 under 35 U.S.C. § 102(e) as anticipated by Yasui et al. Applicant respectfully traverses those rejections for at least the following reasons.

Claim 1

Among other things, claim 1 recites that the gate driver receives a first gate voltage which changes prior to exciting of successive gate signal lines, wherein the first gate voltage has a voltage level that turns on the switching transistor.

For example only, and not by way of limitation, Applicant points the Examiner's attention to the embodiment described with respect to Figs. 5 and 6, where it can be seen that the gate driver 34 receives first (V_{GH}) and second (V_{GL}) gate voltages, wherein the first gate voltage (V_{GH}) changes from V_{DD} to GVL at the falling edge of the gate scanning clock signal GSC prior to exciting the successive gate line at the next rising edge of GSC (see Fig. 6).

Yasui et al. clearly lacks such a feature. As shown in Fig. 2 of Yasui et al., for example, the first gate voltage in Yasui et al. corresponds to V_{GH}, the voltage level of the high-level gate pulse P_G. Applicant respectfully submits that the Examiner has failed to cite any disclosure or suggestion in Yasui et al. that the first gate voltage V_{GH} changes prior to

exciting of successive gate signal lines. Indeed, Figs. 2, 4A-B, 5A-B, 8A-D, etc. of Yasui et al. all indicate that the gate driver 3 merely switches from providing the first gate voltage V_{GH}, to providing the second gate voltage V_{GL}, coincident with, or prior to, exciting successive gate signal lines (see also col. 15, lines 1-14).

Applicant respectfully submits that the Examiner has fairly admitted the same in the Final Rejection mailed on 14 February 2001:

> "*Yasui et al. teaches all of the claimed limitations of claim 1, except for the first gate voltage drop prior to exciting of the successive gate signal lines, exponentially, linearly and stepwise*"

Office Action dated 14 February 2001, at page 4, lines 3-5.

Accordingly, with Yasui et al. admittedly failing to include a recited element of claim 1, Applicant respectfully submits that Yasui et al. cannot anticipate the claimed invention under 35 U.S.C. § 102(e). Therefore, Applicant respectfully requests that the Examiner withdraw his rejection and allow claim 1.

Claim 7

Claim 7 recites a method of driving an active matrix liquid crystal display apparatus which includes, among other things, a step of supplying a first gate voltage and a second gate voltage, selectively via a switching device, to the gate lines, said switching device being controlled by a shift register, wherein the first gate voltage varies before the second gate voltage is supplied to the gate lines. For example only, and not by way of limitation, Applicant again points the Examiner's attention to the embodiment described with respect to

Figs. 5 and 6, where it can be seen that the switching device 39 receives first (V_{GH}) and second (V_{GL}) gate voltages, wherein the first gate voltage (V_{GH}) varies from V_{DD} to GVL by means of switch 50 at the falling edge of the gate scanning clock signal GSC before the second gate voltage (V_{GL}) is supplied to the gate line by the switch 39.

Yasui et al. clearly lacks such a feature. As shown in Fig. 2 of Yasui et al., for example, the first gate voltage corresponds to V_{GH}, the voltage level of the high-level gate pulse P_G, and the second gate voltage corresponds to V_{GL}. Applicant respectfully submits that the Examiner has failed to cite any disclosure or suggestion in Yasui et al. that the first gate voltage V_{GH} varies before the second gate voltage V_{GL} is applied to the gate line. Indeed, Figs. 2, 4A-B, 5A-B, 8A-D, etc. of Yasui et al. all indicate that the gate driver 3 switches from the first gate voltage V_{GH} to the second gate voltage V_{GL} without providing for any variation in the first gate voltage V_{GH}.

Accordingly, Yasui et al. cannot possibly anticipate the invention of claim 7 under 35 U.S.C. § 102(e). Therefore, Applicant respectfully requests that the Examiner withdraw his rejection and allow claim 7.

Claims 8-9, dependent from claim 7, are deemed to be similarly allowable.

35 U.S.C. § 103

The Examiner rejected claims 2-6 under 35 U.S.C. § 103 as unpatentable over Yasui et al. in view of Suzuki et al. Applicant respectfully traverses those rejections for at least the following reasons.

Among other things, Suzuki et al., like Yasui et al, fails to disclose or suggest a gate driver receives a first gate voltage which changes prior to exciting of successive gate signal

lines, wherein the first gate voltage has a voltage level that turns on the switching transistor. Applicant respectfully submits that the Examiner has not stated that Suzuki et al. includes such an element, and indeed it does not include such an element. Accordingly, as at least this one element of the claimed invention is missing from both Suzuki et al. and Yasui et al, no possible combination of Suzuki et al. and Yasui et al can produce the present invention of claims 2-6 which includes such an element. Therefore, Applicant respectfully requests that the Examiner withdraw his rejections and allow claims 2-6.

New Claims 10-15

Claims 10-15 each depend from claim 1 and are deemed allowable for at least the reason set forth above with respect to claim 1, and the for at least the following additional reason.

Among other things, each of the claims 10-15 includes a feature that a high level gate voltage generator provides the first gate voltage to the gate driver, the high level gate voltage generator comprising, a high level voltage source providing a high level voltage, and a voltage controller receiving the high level voltage and providing therefrom the first gate voltage changing prior to exciting of successive gate signal lines.

The prior art references alone and in combination fail to disclose or suggest such a high level gate voltage generator. Accordingly, for at least this additional reason, Applicant respectfully submits that claims 10-15 are allowable.

New Claims 16-20

Among other things, new claims 16-20 include a feature that a driver connected to the

plurality of scanning signal lines receives first and second control voltages and a scanning clock signal and, in response to the scanning clock signal, successively outputs the first control voltage to the scanning signal lines to sequentially drive the scanning signal lines, wherein the voltage level of the first control voltage received by the driver changes during a period of the scanning clock signal prior to the driver selecting a successive scanning line.

None of the cited prior art references, alone or in combination, include or suggest such a feature. Accordingly, Applicants respectfully submit that claims 16-20 are allowable.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911 (8733.164.2). Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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Date: July 13, 2001

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